High-Performance Scientific Computing
Lecture 3: OpenCL

MATH-GA 2011 / CSCI-GA 2945 · September 19, 2012

Today

HW2

Chips for Throughput

Synchronization

Admin Bits

- New here? Please send email

Admin Bits

- New here? Please send email
- Started looking for a final project yet?

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- HW1 not found $\rightarrow$ email

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- Overall pace
- HW3 out on the weekend

Outline

HW2 problem 2

Demo time

OpenMP sync primitives

- Critical section

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- Locks

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- Atomics

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- Atomics
  - Update: `x++;`
  - Capture: `v = x++;`
  - Structured: v = x; x —= expr; ("Test-and-set")
  - Compare-and-swap (not in OpenMP)

OpenMP corner case pop quiz 1

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- May OpenMP directives be nested?
  - What is an orphaned directive?
  - What is close nesting?
  - What is a 'dynamic extent' of a region?
- May a worksharing region be closely nested inside another one?
- What happens if I nest two `critical` regions of the same name?

OpenMP corner case pop quiz 2

- Corresponding getter function for `omp_set_num_threads()`?

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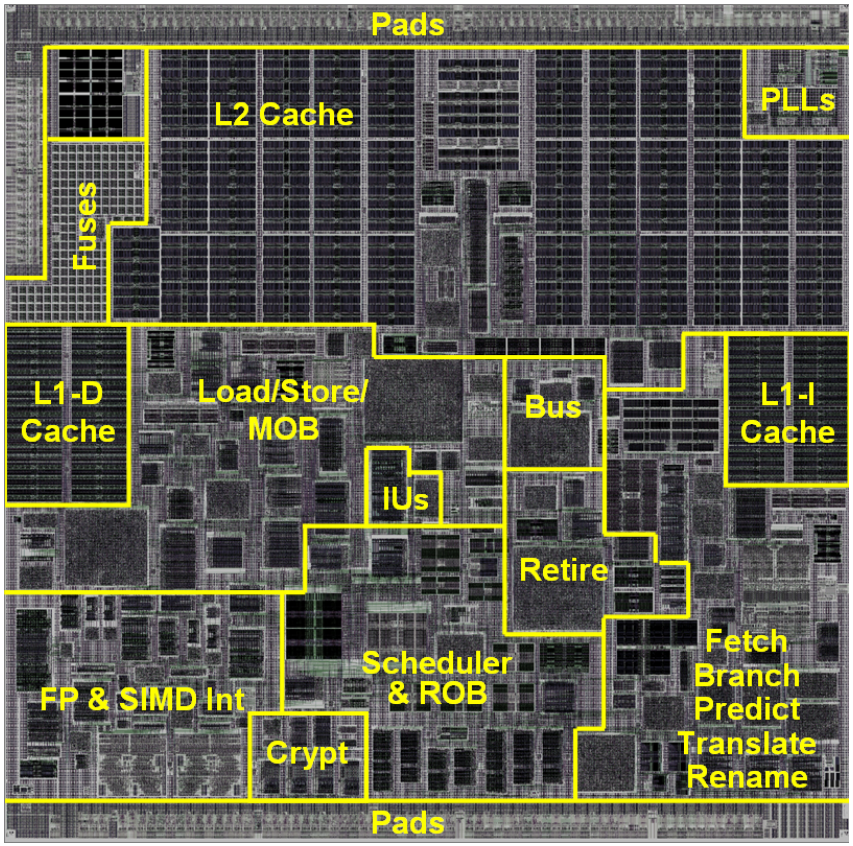
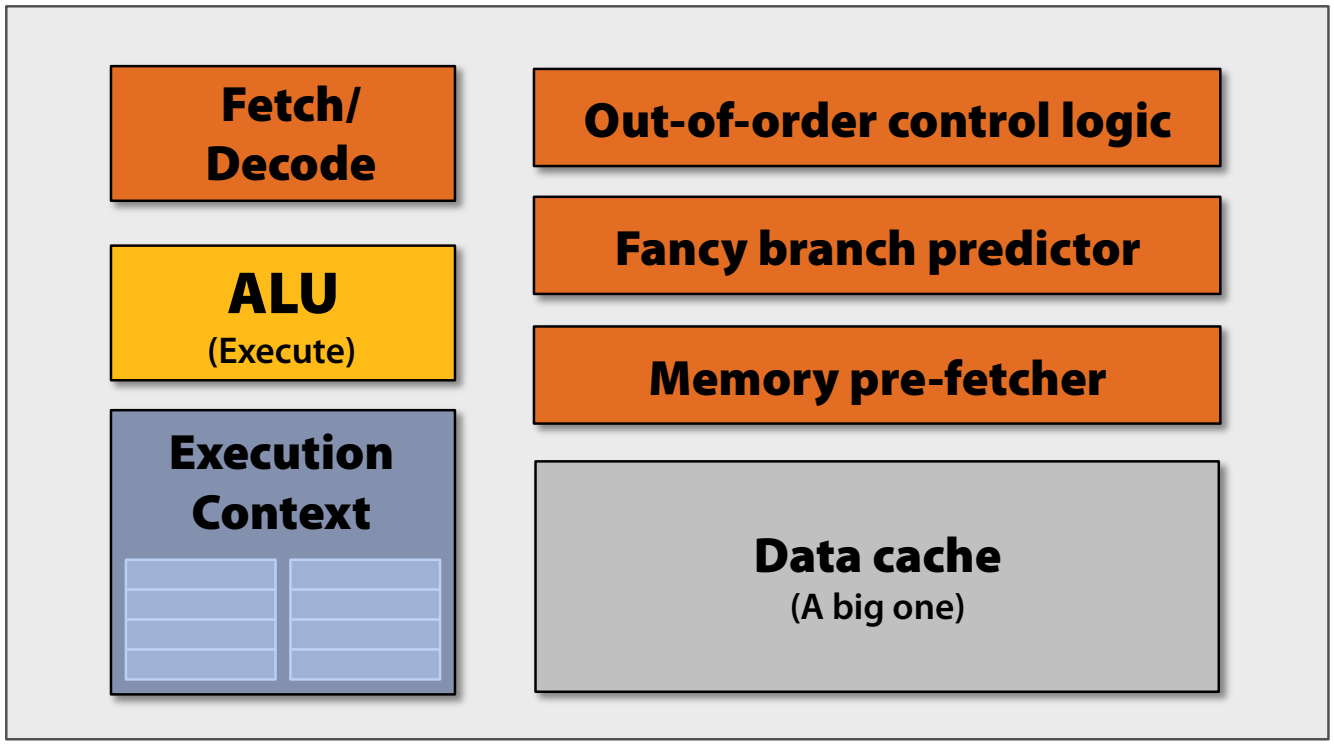
Outline

CPU Chip Real Estate



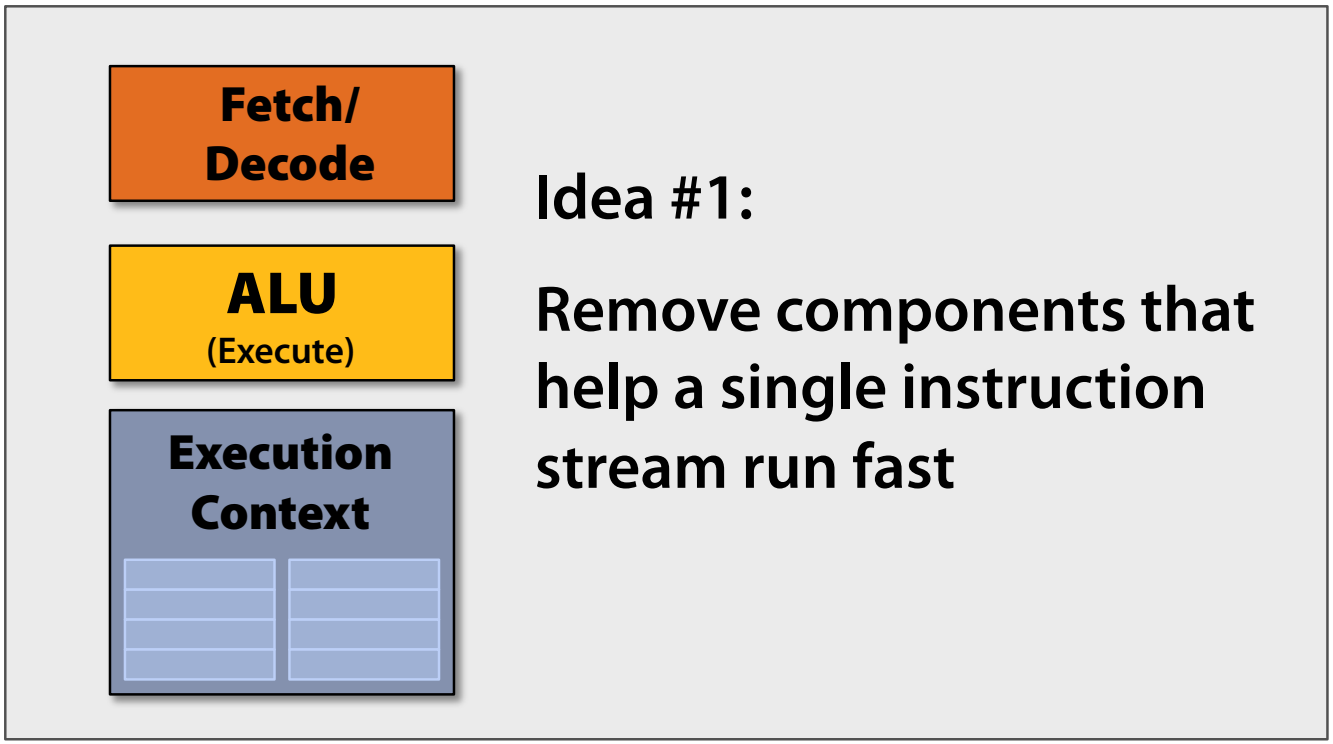
Die floorplan: VIA Isaiah (2008).
65 nm, 4 SP ops at a time, 1 MiB L2.

"CPU-style" Cores



Credit: Kayvon Fatahalian (Stanford)

Slimming down



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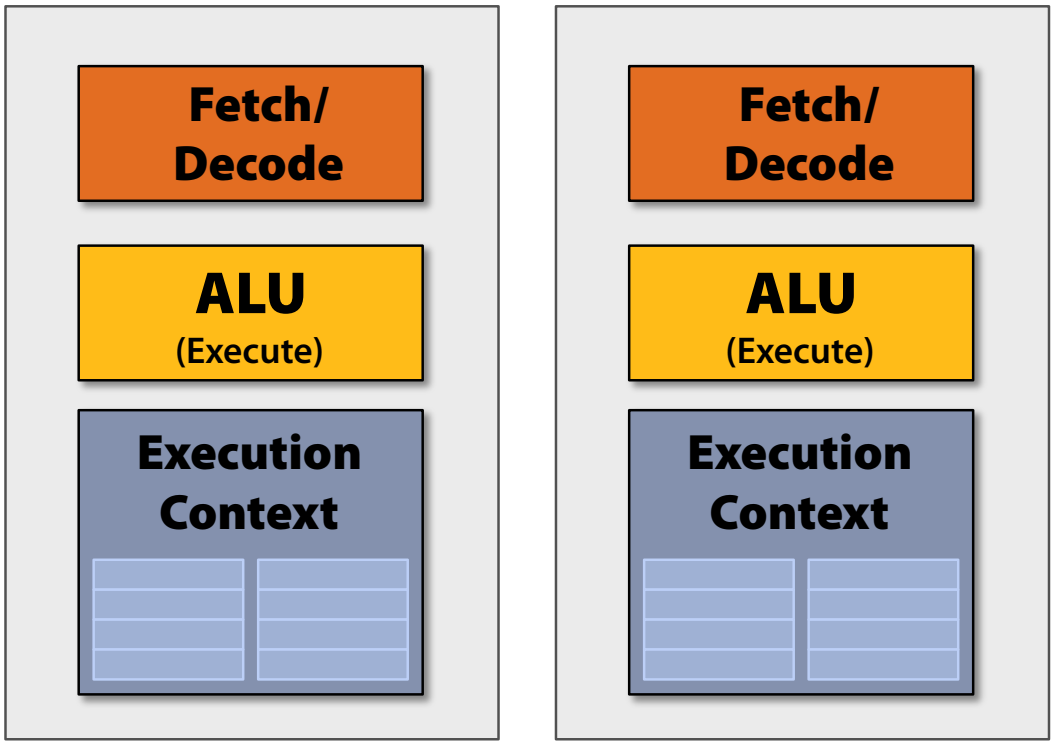
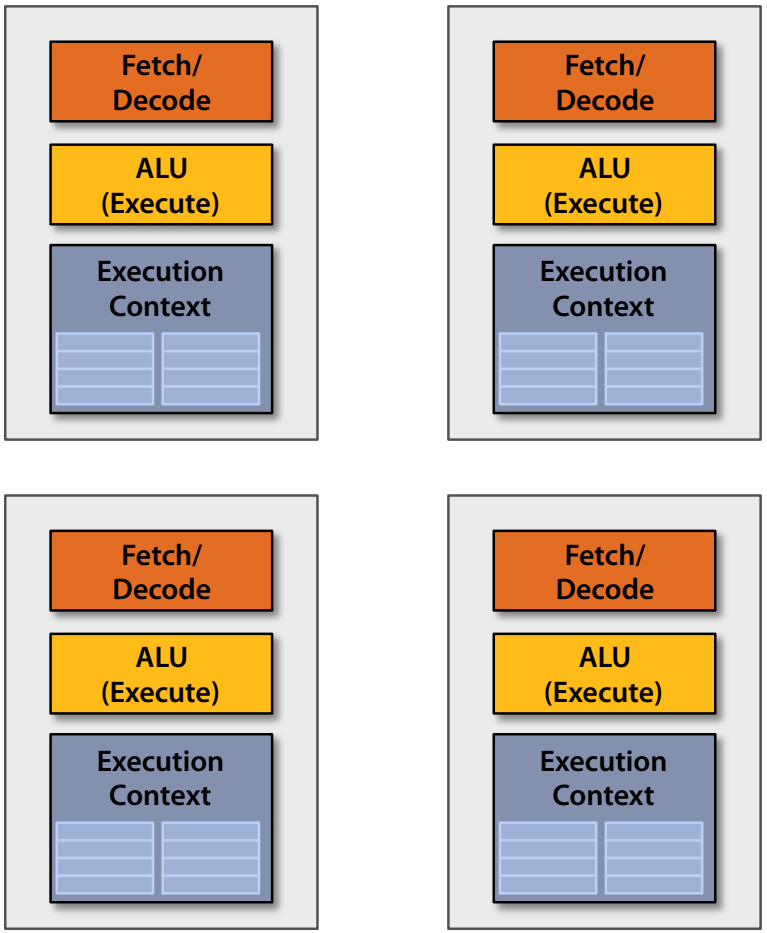
More Space: Double the Number of Cores



Credit: Kayvon Fatahalian (Stanford)

. . . again



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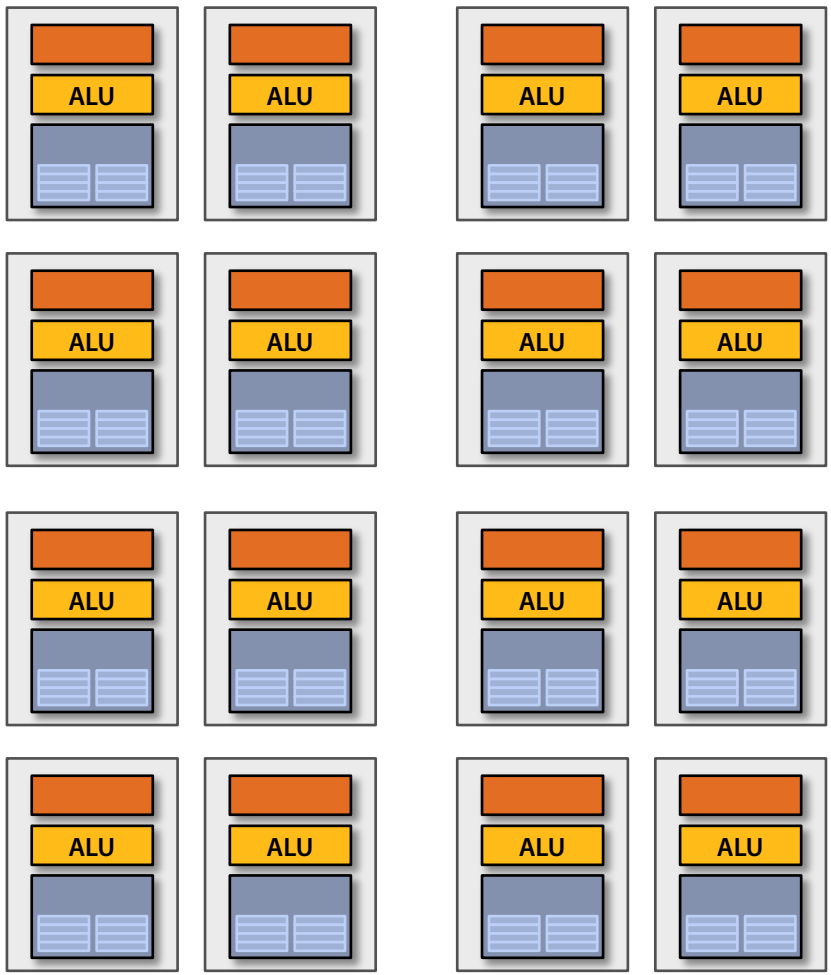

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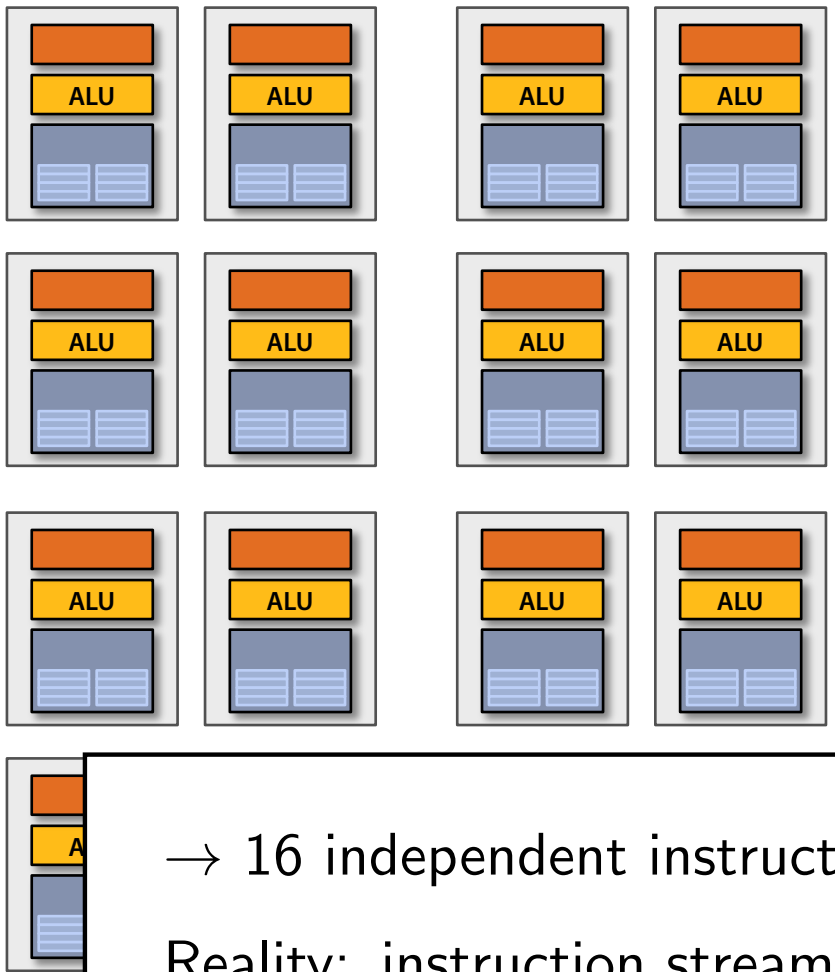
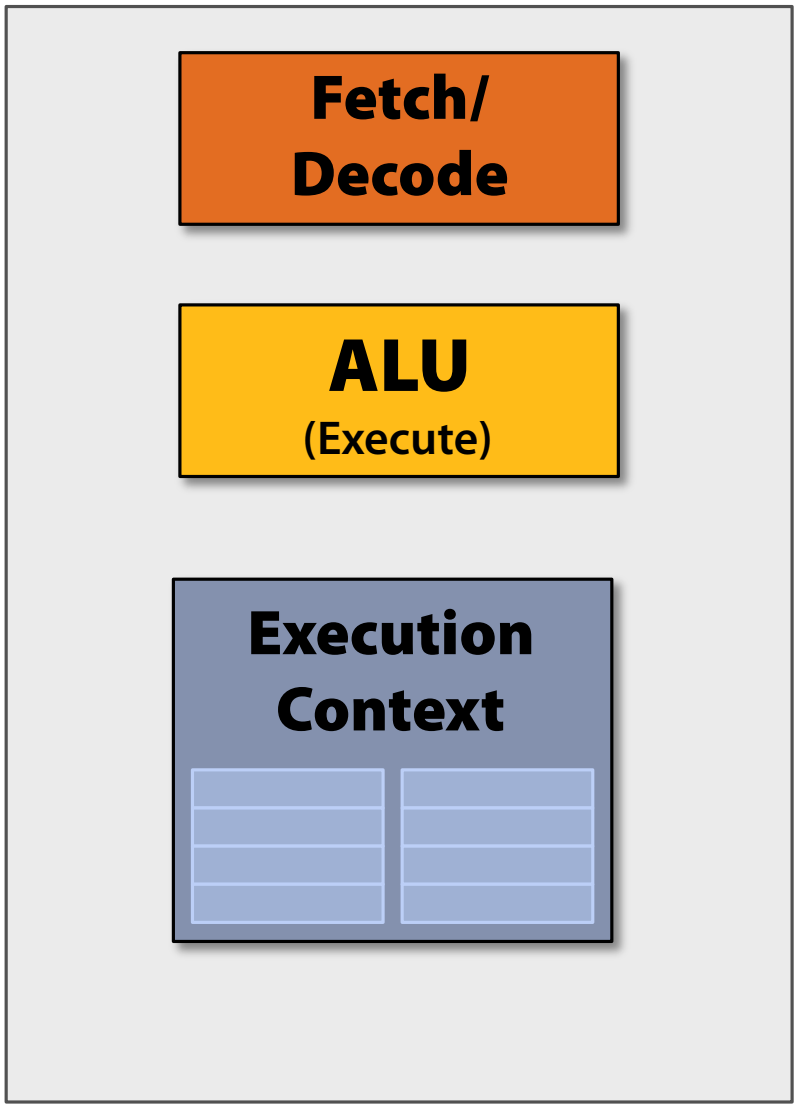


→ 16 independent instruction streams

Reality: instruction streams not actually very different/independent

Credit: Kayvon Fatahalian (

Saving Yet More Space



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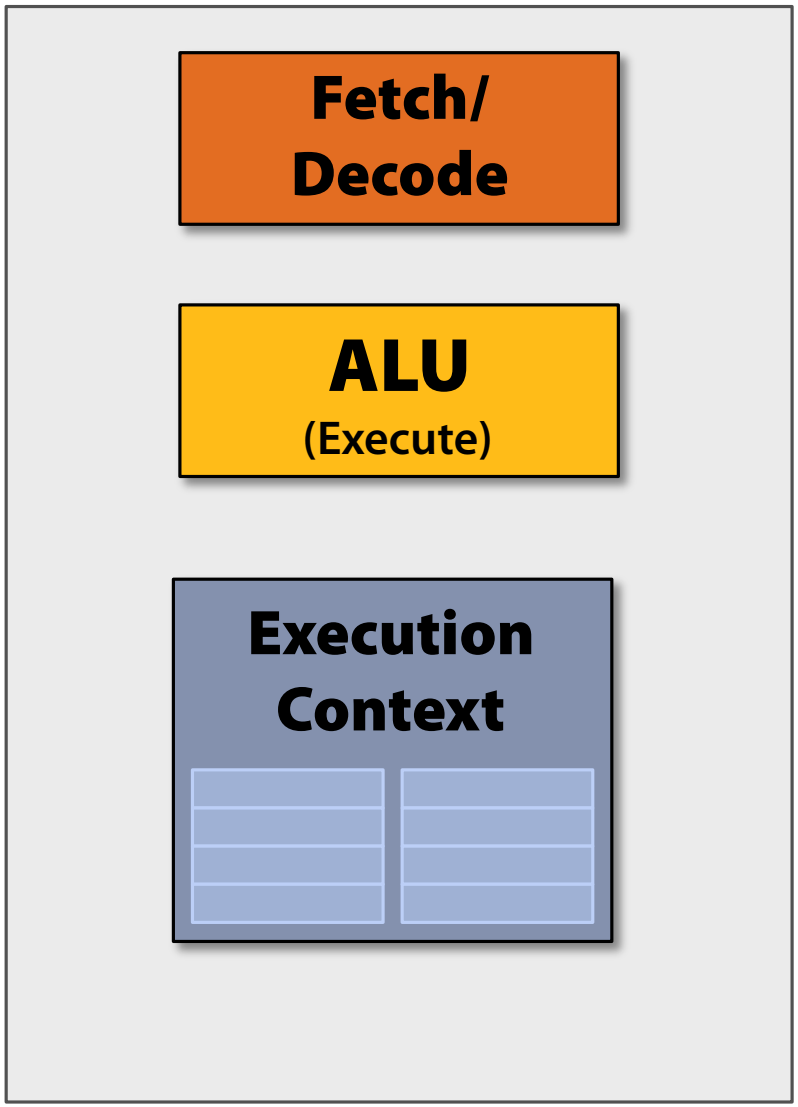

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Idea #2

Amortize cost/complexity of managing an instruction stream across many ALUs

→ **SIMD**

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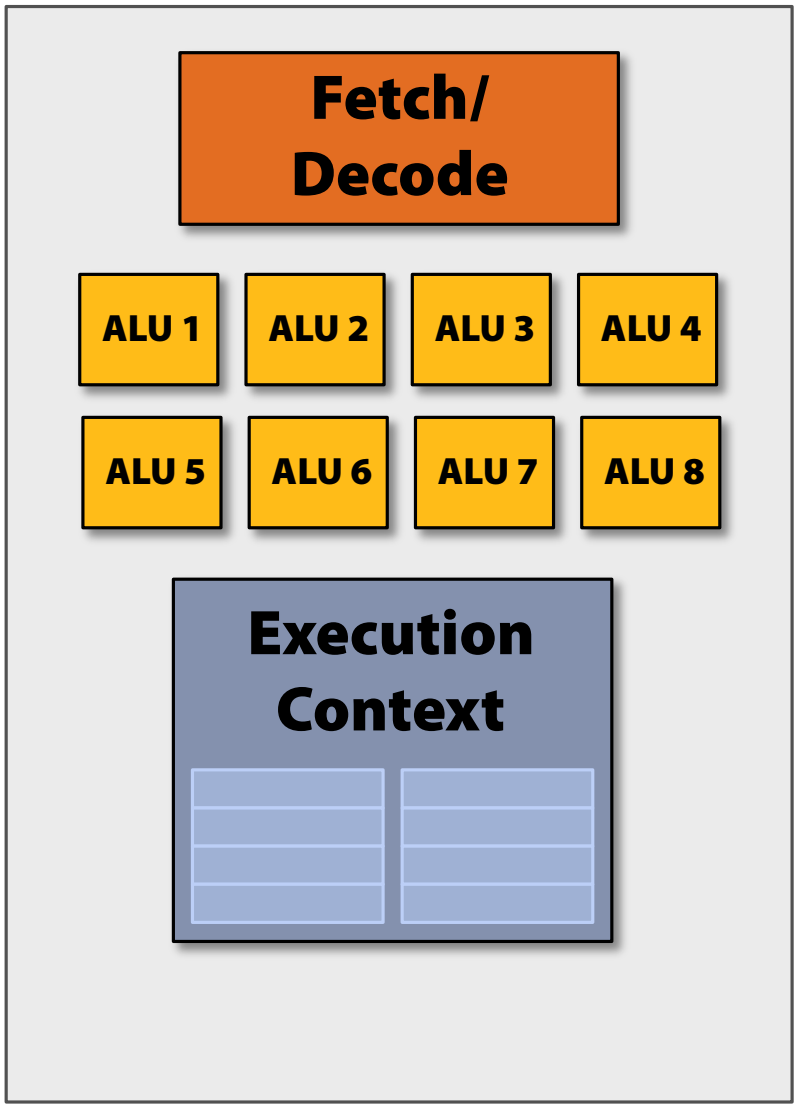

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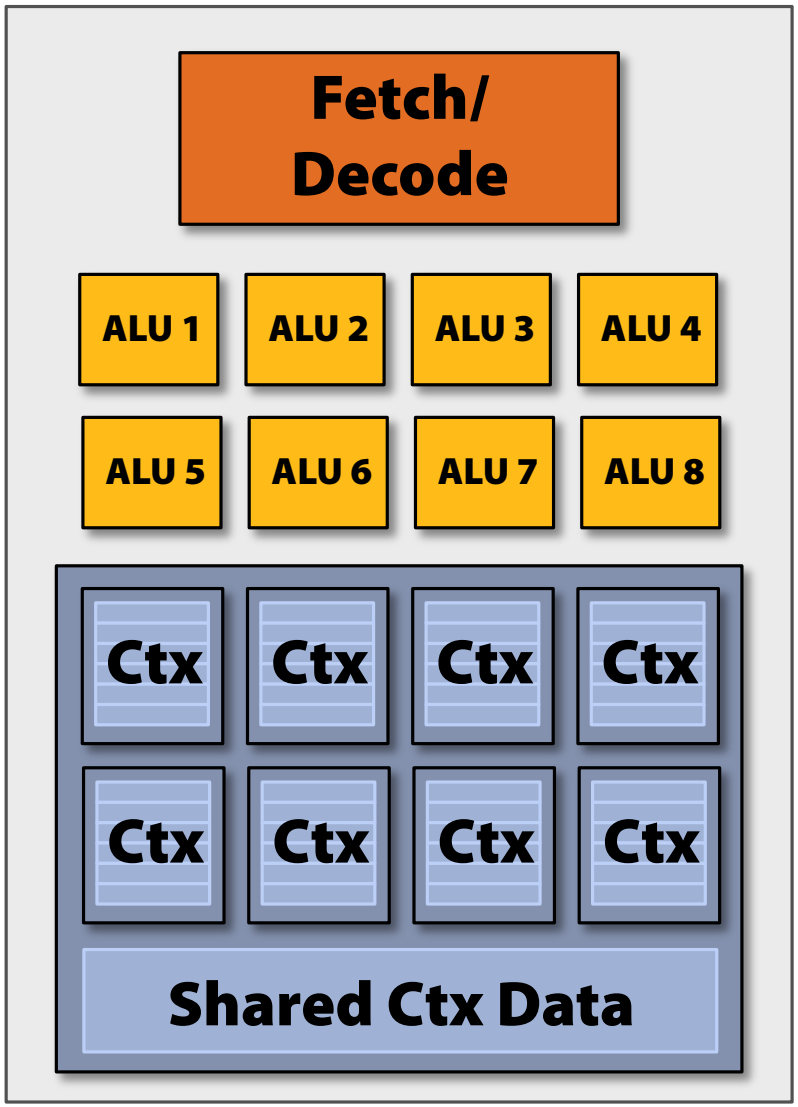

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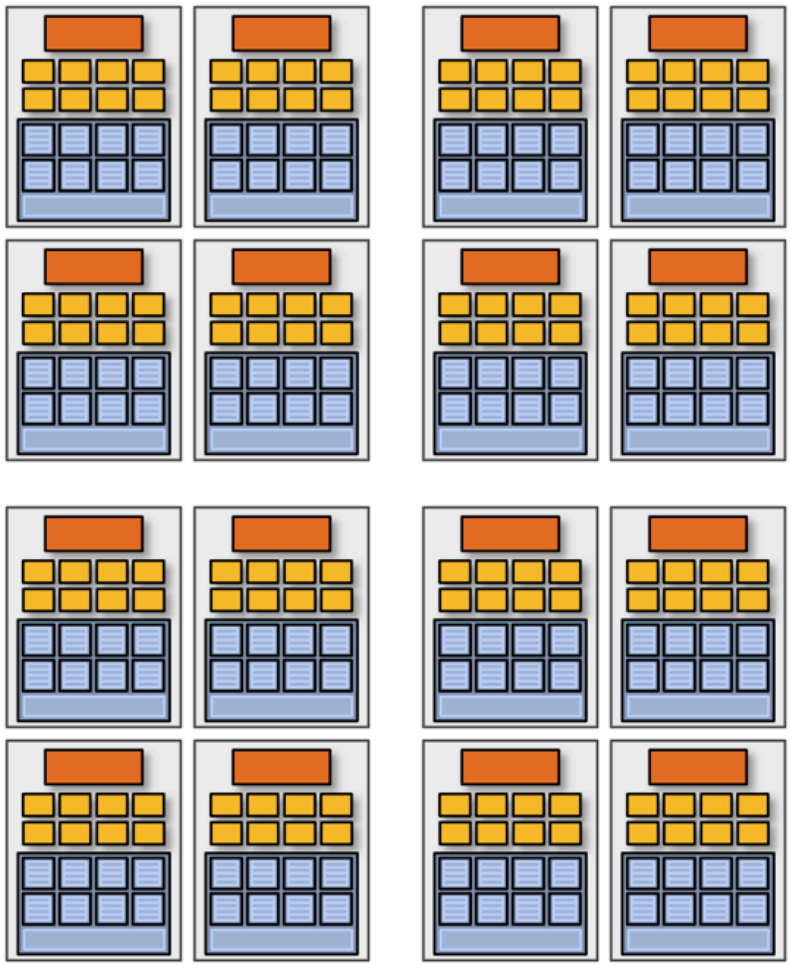
Gratuitous Amounts of Parallelism!



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Gratuitous Amounts of Parallelism!

Example:

128 instruction streams in parallel
16 independent groups of 8 synchronized streams

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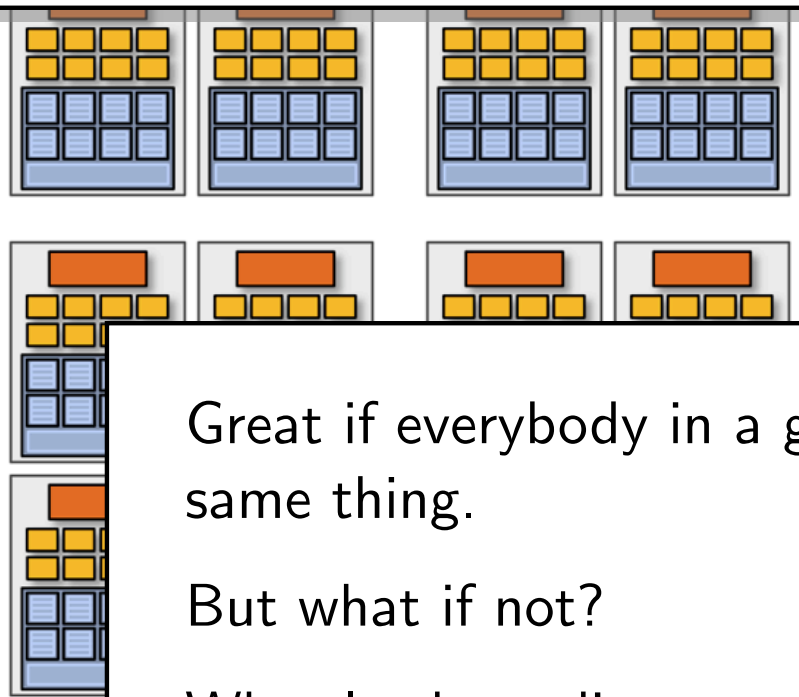


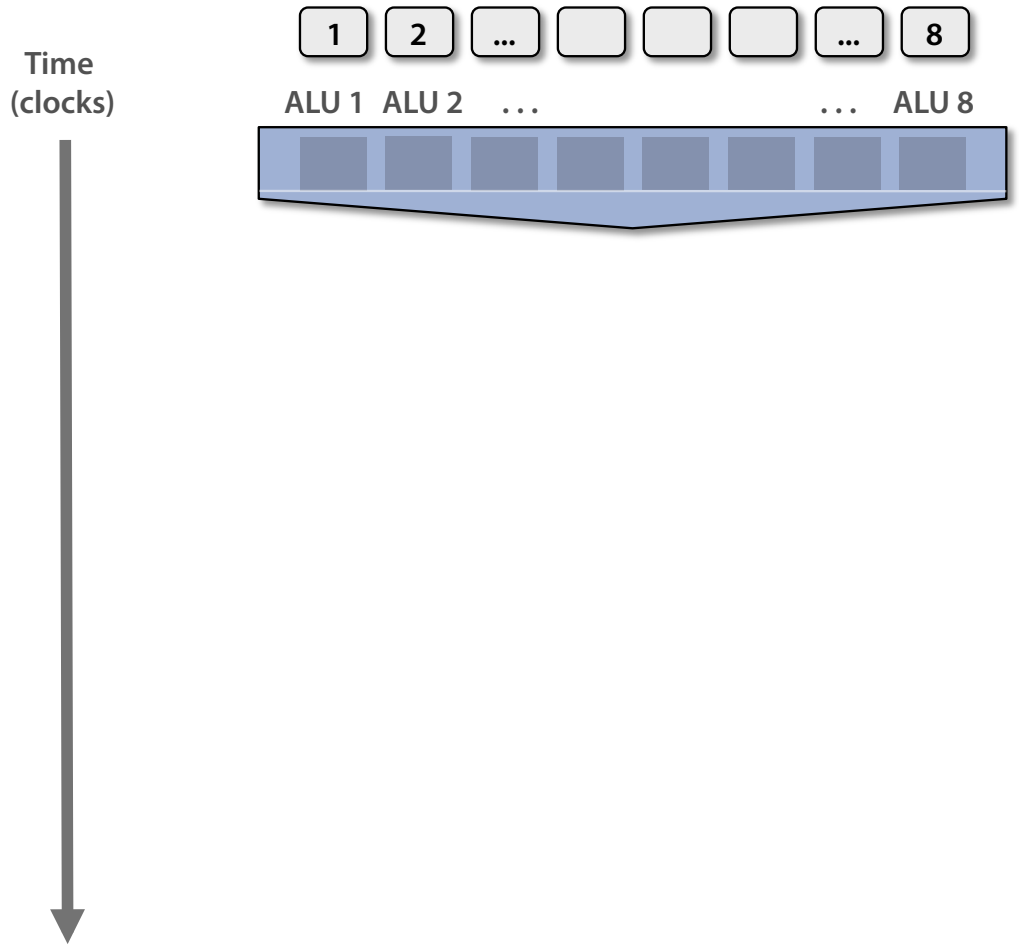
Great if everybody in a group does the same thing.

But what if not?

What leads to divergent instruction streams?

Credit: Kayvon Fatahalian (

Branches

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<unconditional
shader code>

if (x > 0) {
    y = pow(x, exp);
    y *= Ks;
    refl = y + Ka;
} else {
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Credit: Kayvon Fatahalian (Stanford)

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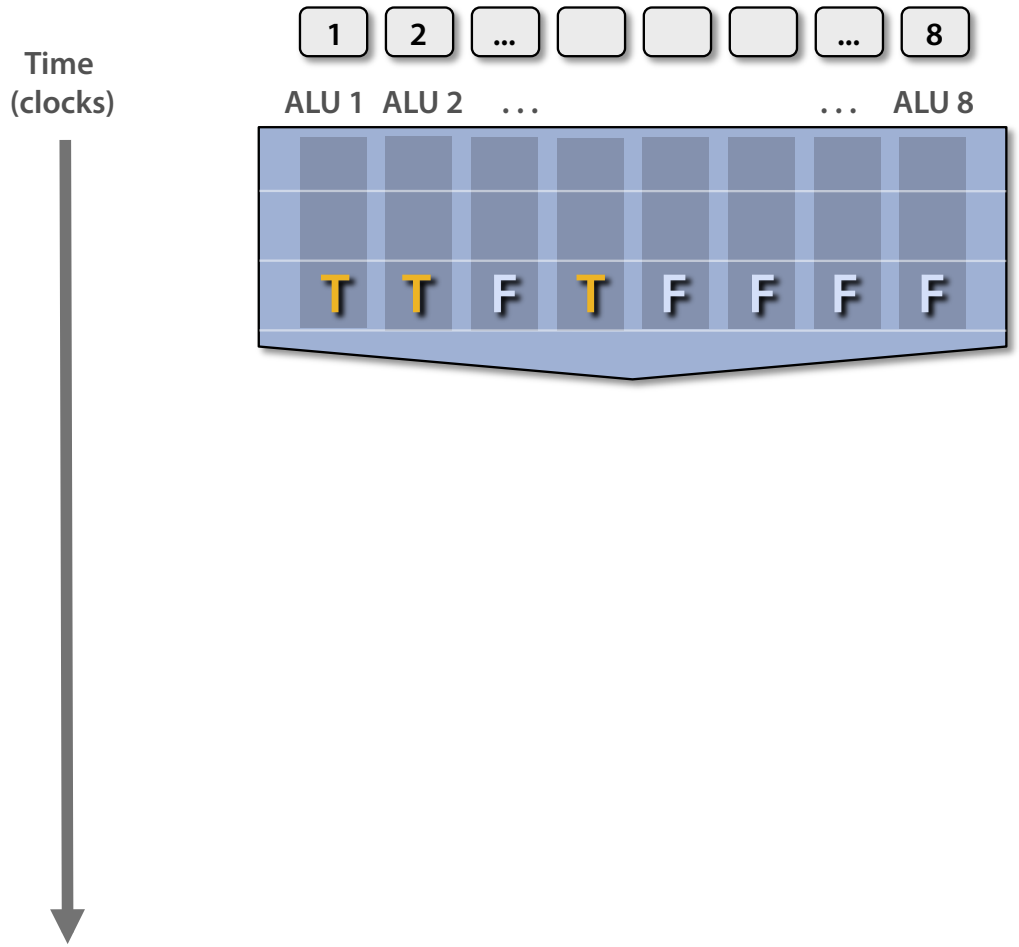


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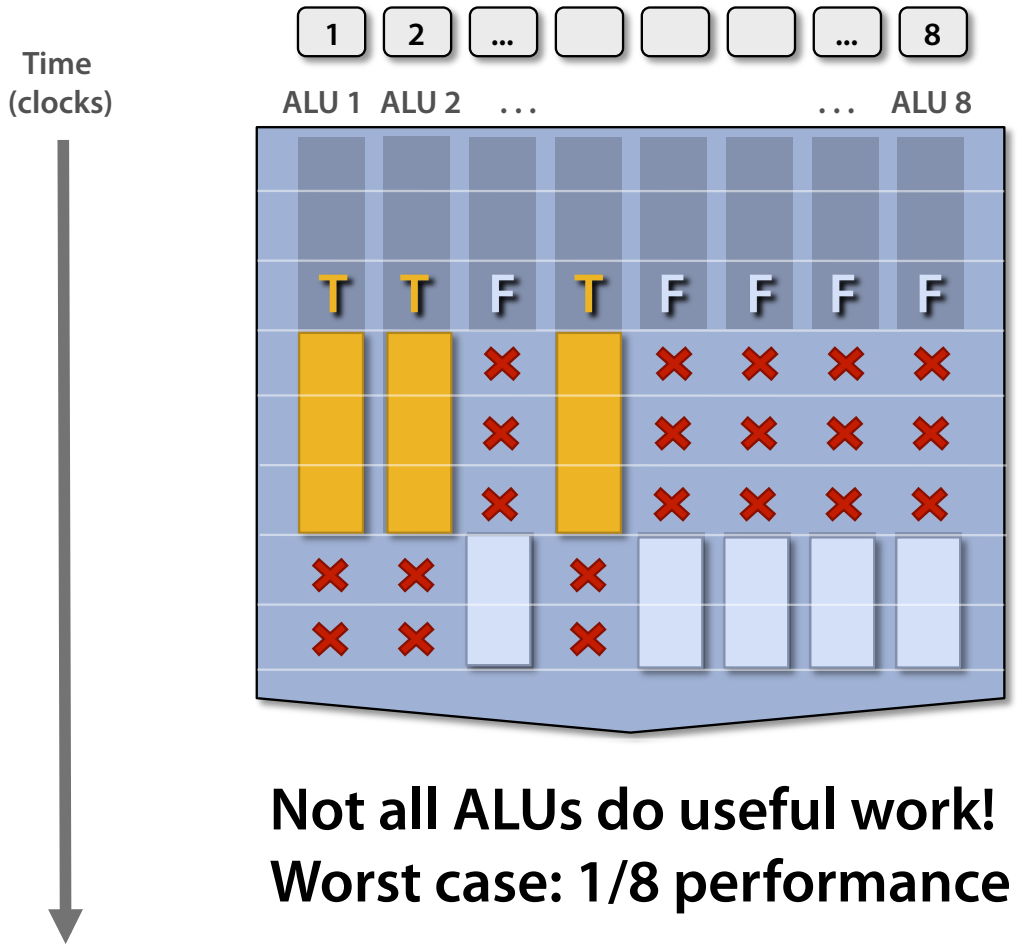

Not all ALUs do useful work!
Worst case: 1/8 performance

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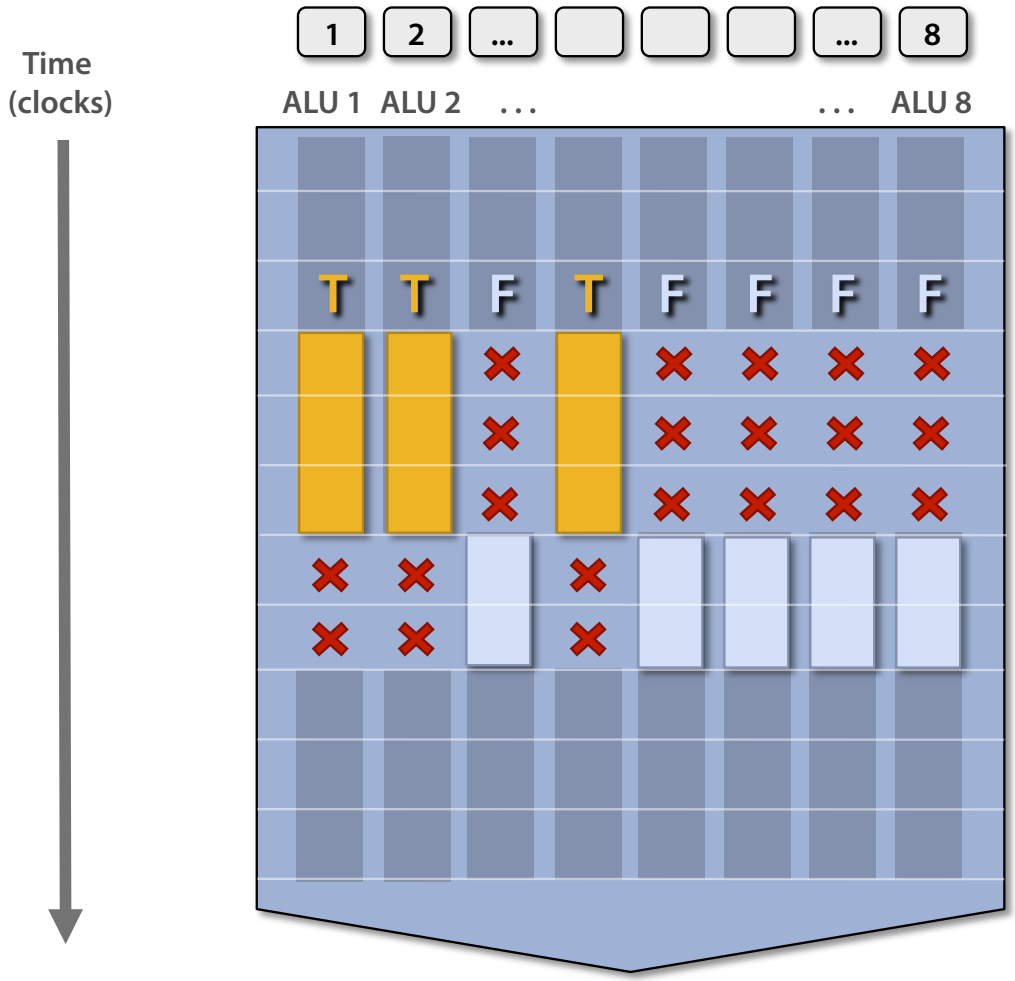


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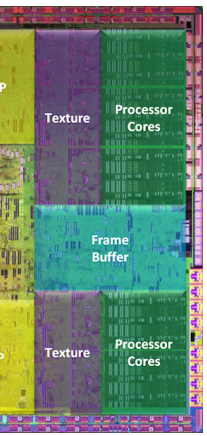
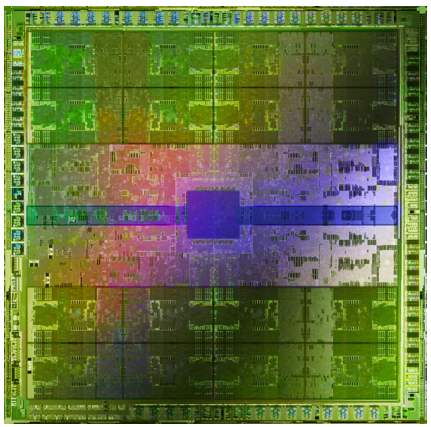
Recent Processor Architecture

- Commodity chips
- "Infinitely" many cores
- "Infinite" vector width
- Must hide memory latency
  ($\rightarrow$ ILP, SMT)

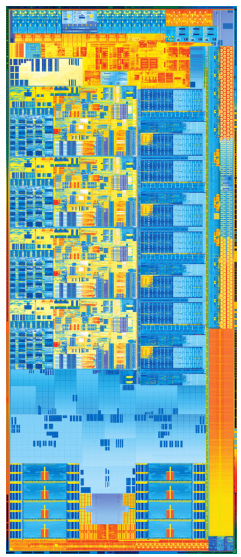
- Compute bandwidth
  $\gg$ Memory bandwidth
- Bandwidth only achievable
  by *homogeneity*



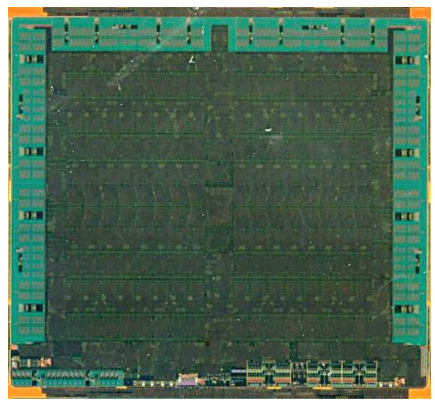
T200
08)



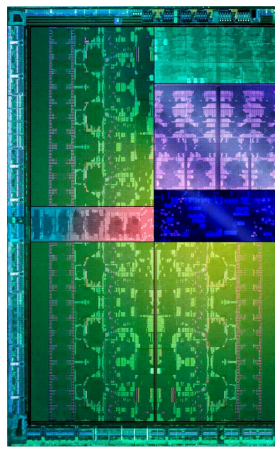
Nv Fermi
(2010)



Intel IVB
(2012)



AMD Tahiti
(2012)



Nv GK1
(2012

Outline

Synchronization

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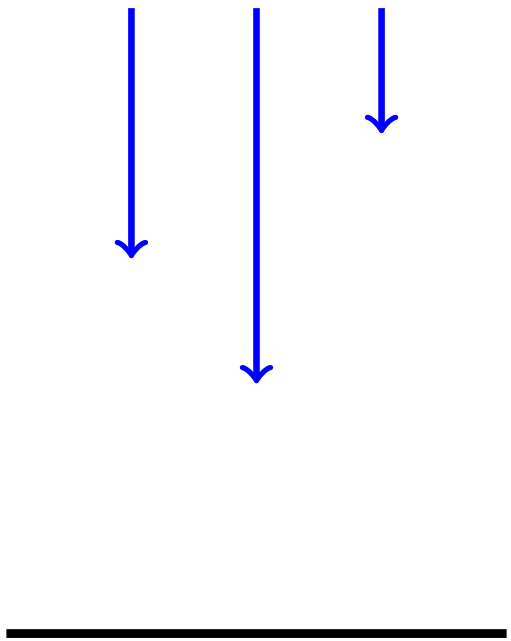

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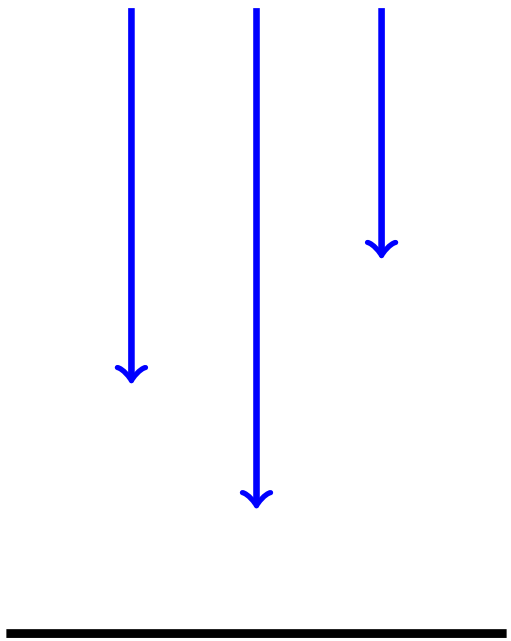

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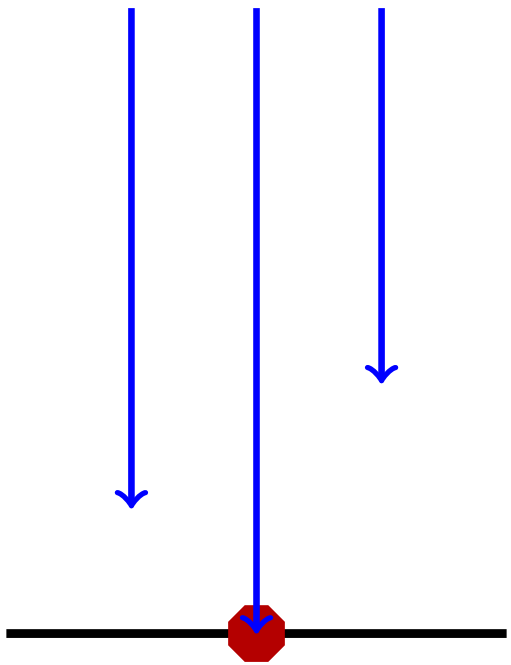

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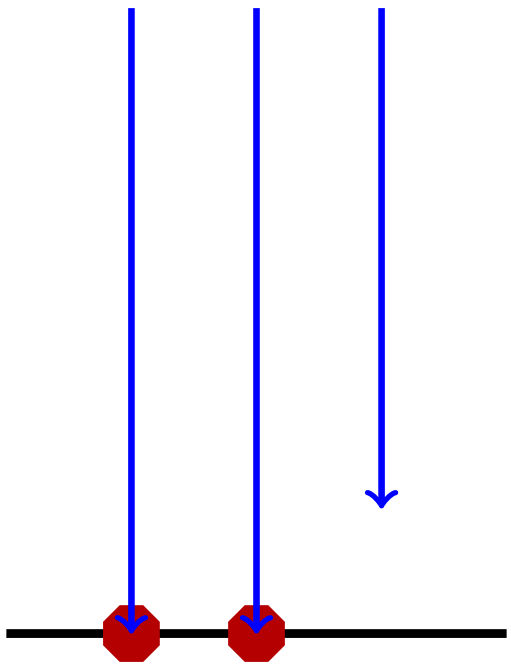

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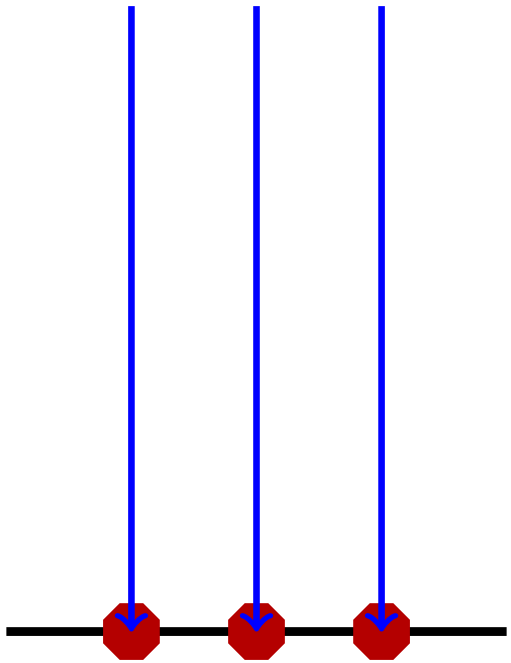

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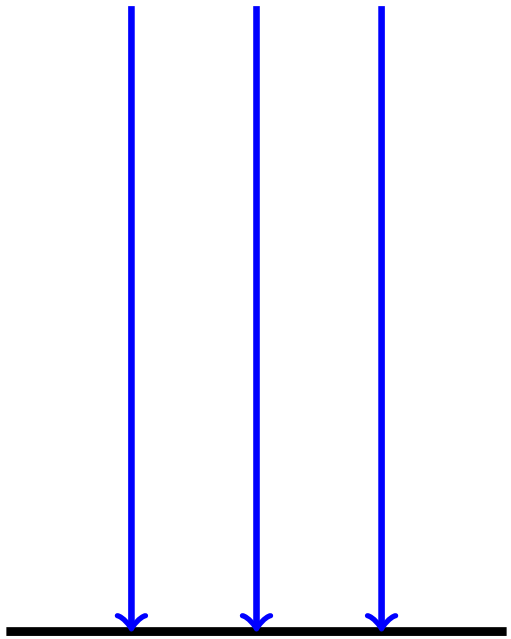

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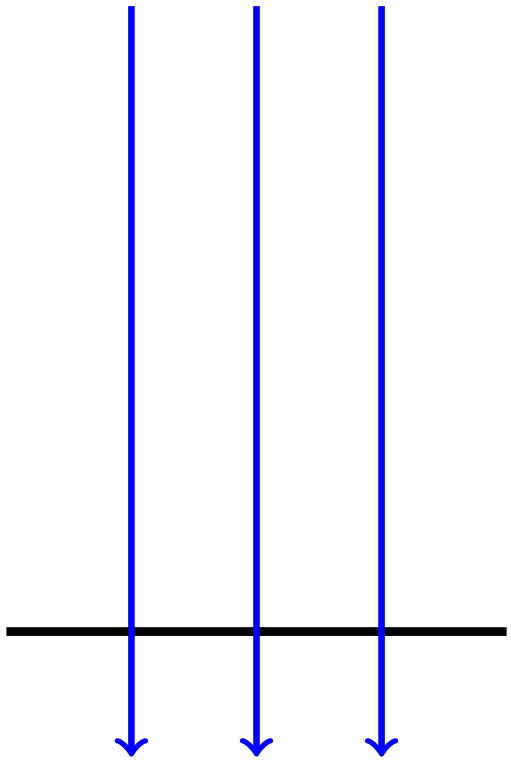
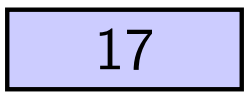


Synchronization

What is a Memory Fence?



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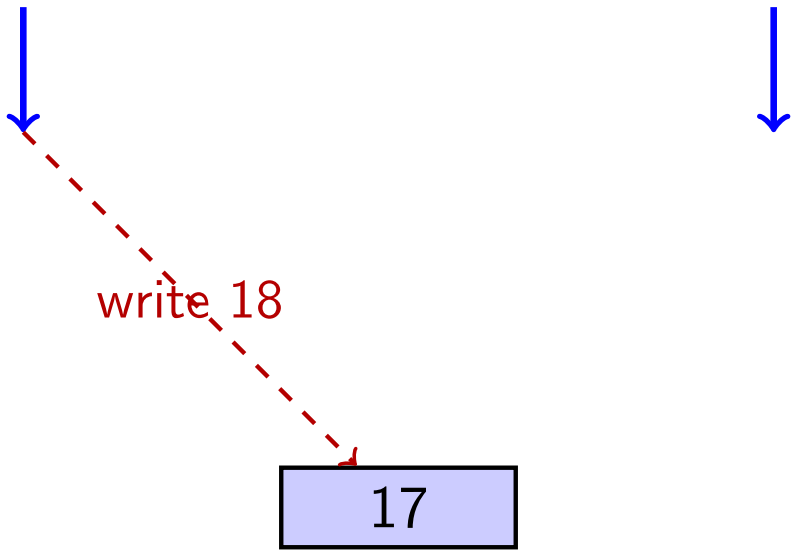

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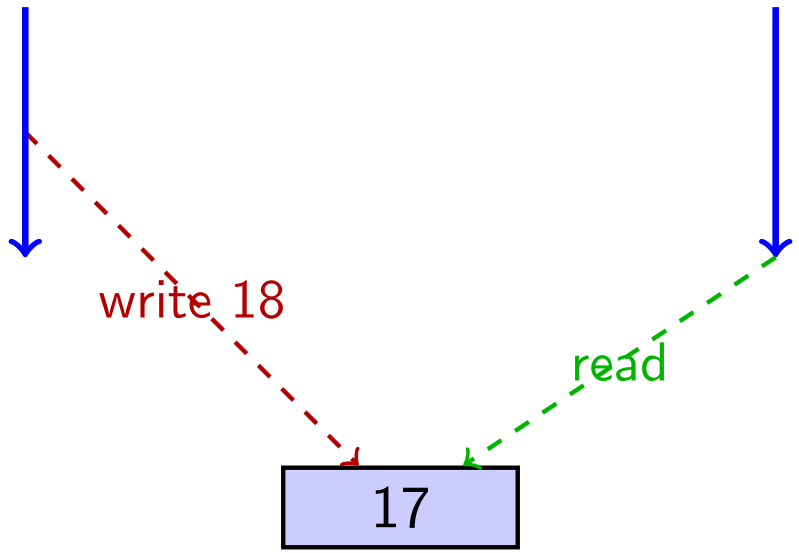

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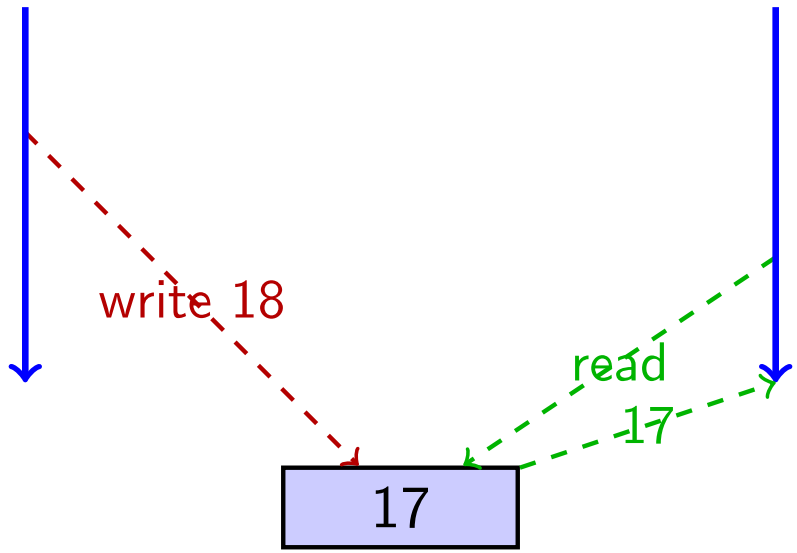

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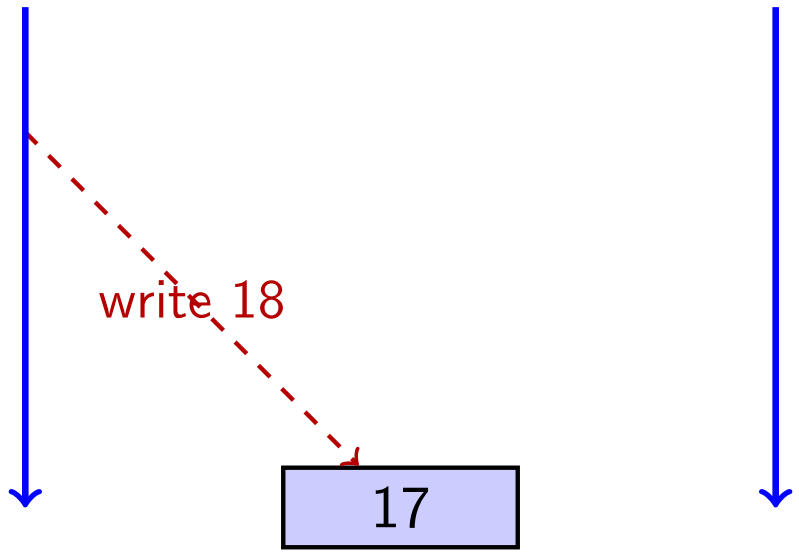

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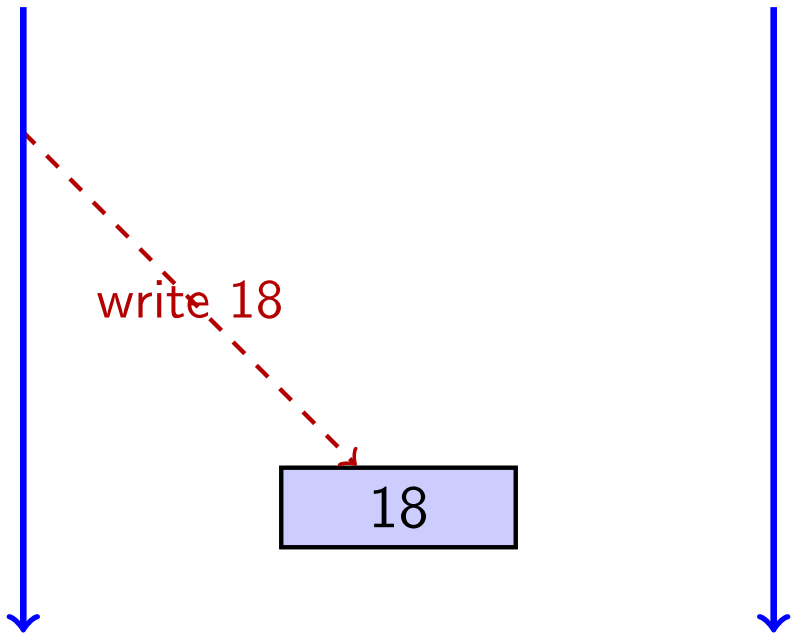

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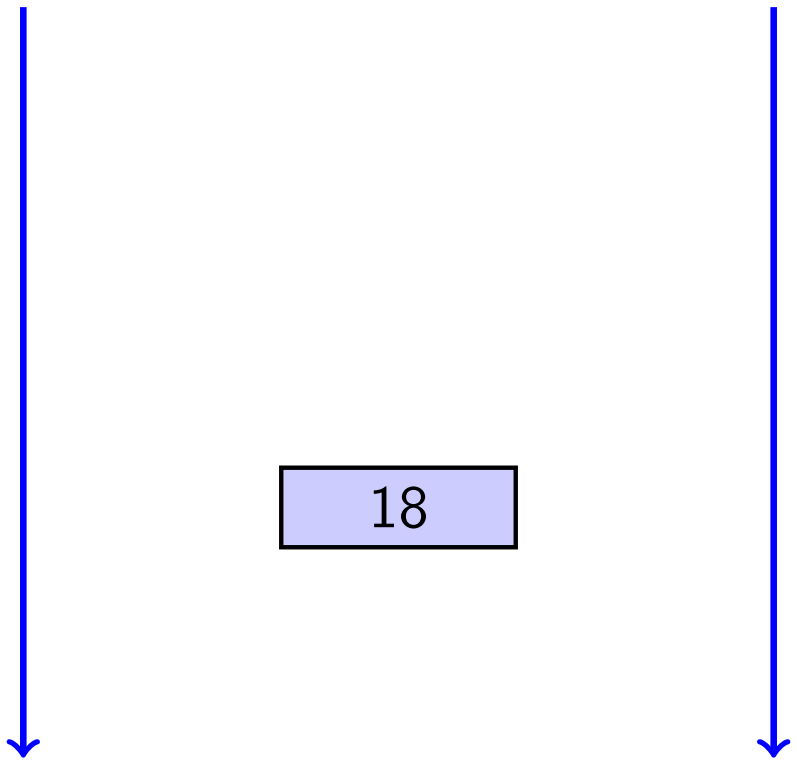
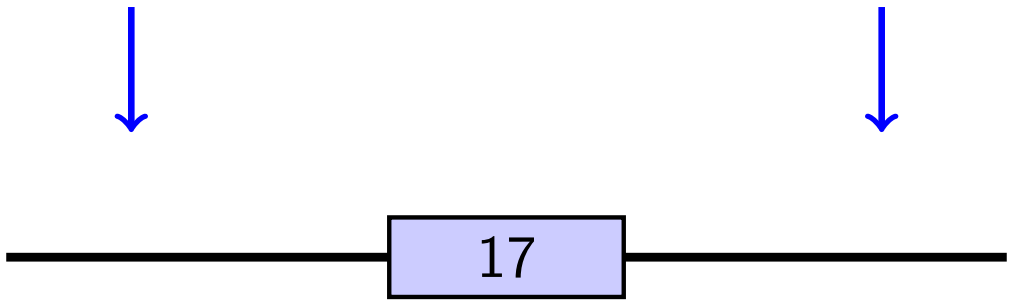


Synchronization

What is a Memory Fence? An ordering restriction for memory access.



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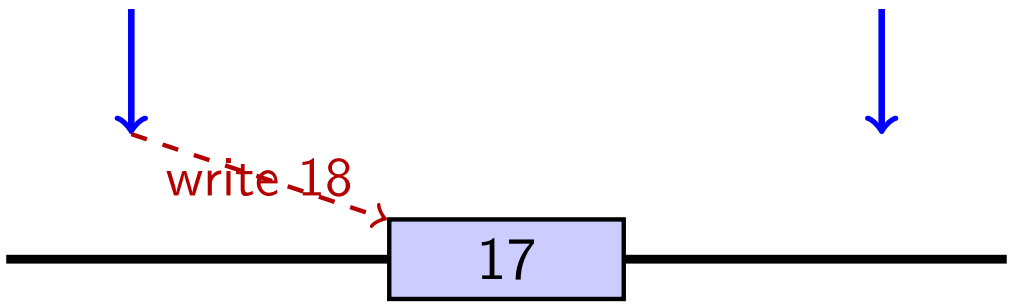

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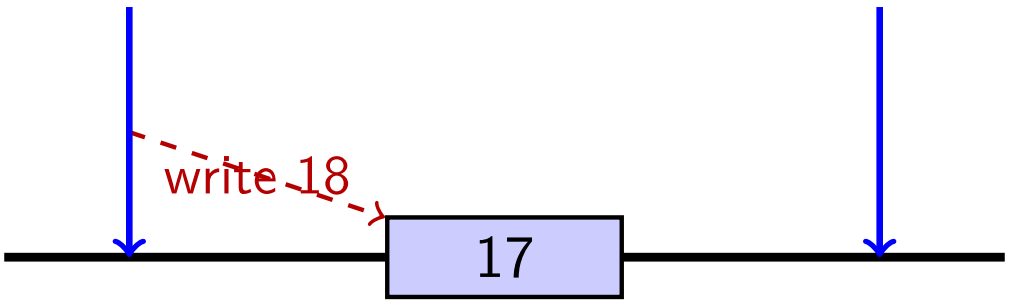

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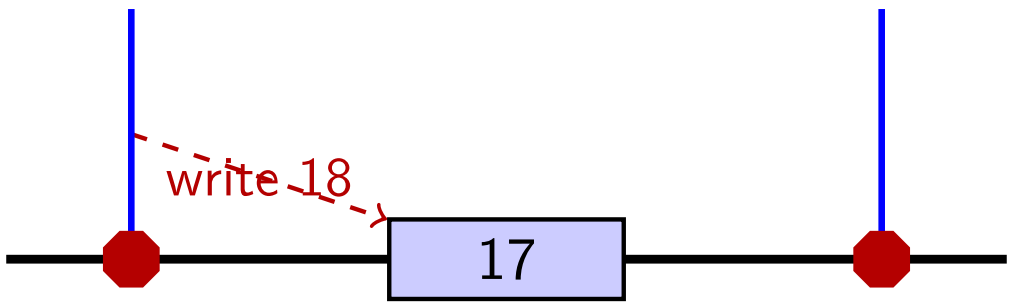

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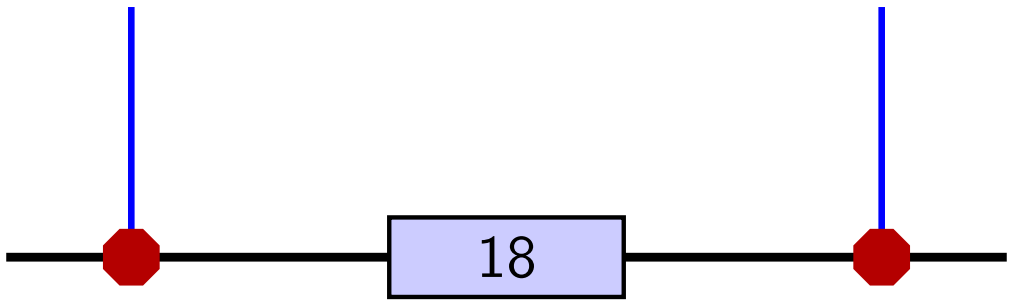

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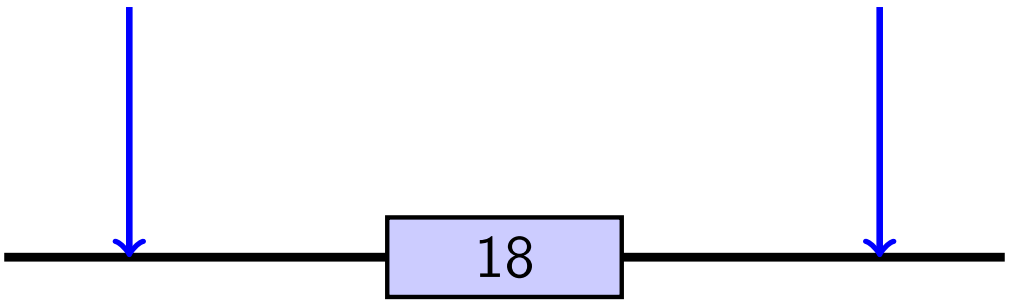

Synchronization

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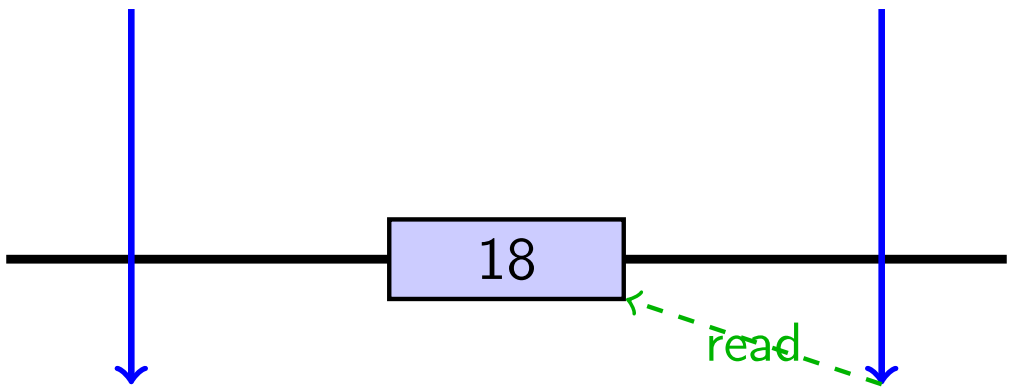

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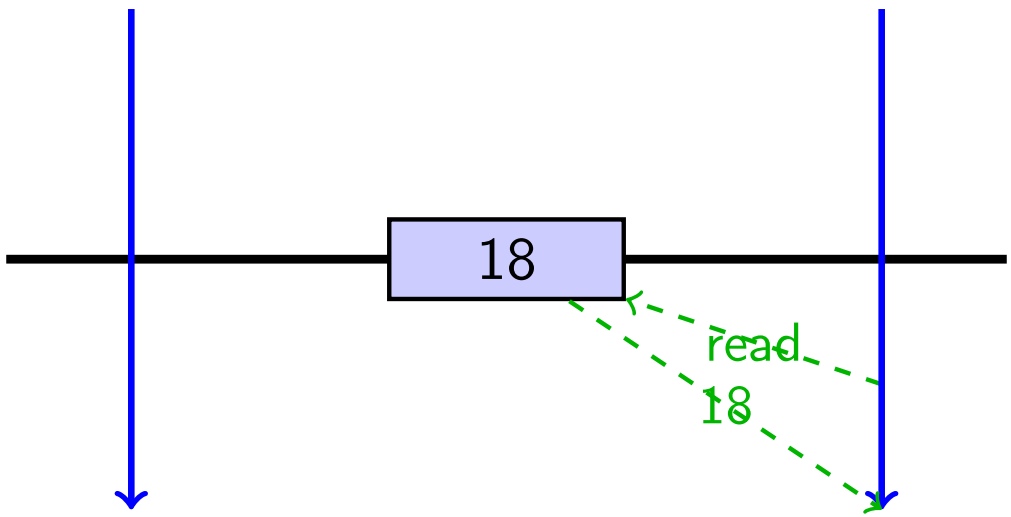

Atomic Operations

Collaborative (inter-block) Global Memory Update:

Atomic Operations

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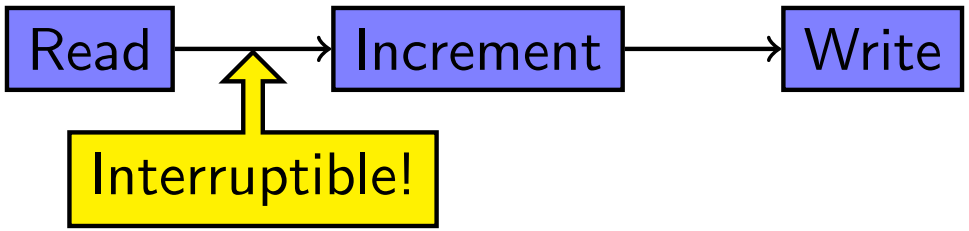

Atomic Operations

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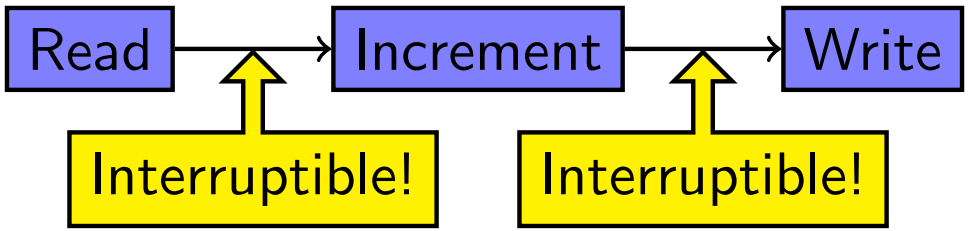

Atomic Operations

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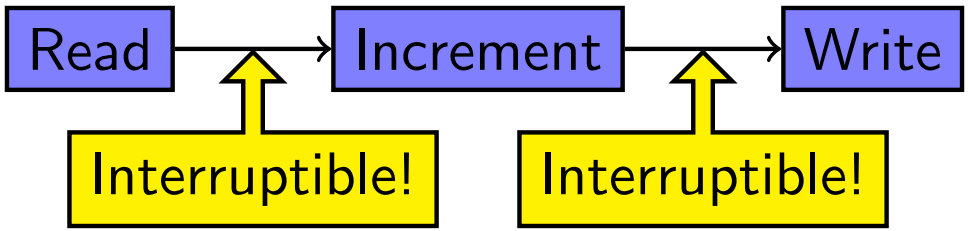

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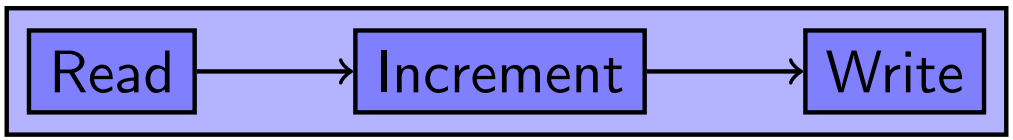

Atomic Operations

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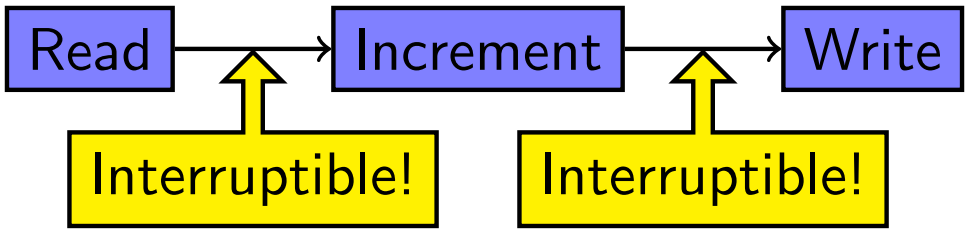

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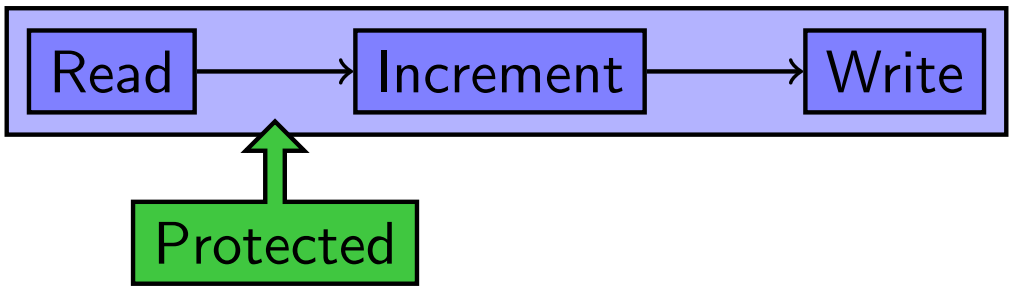

Atomic Operations

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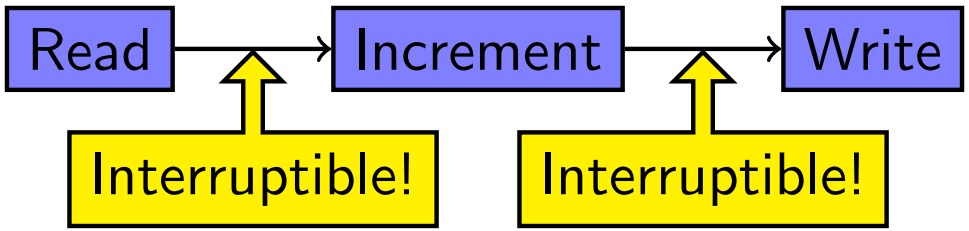

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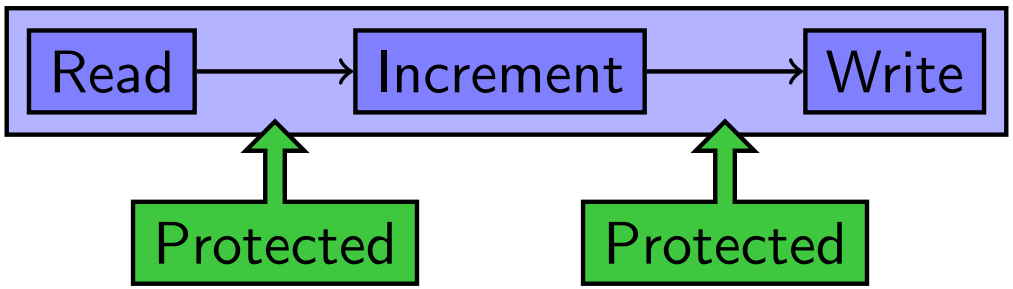

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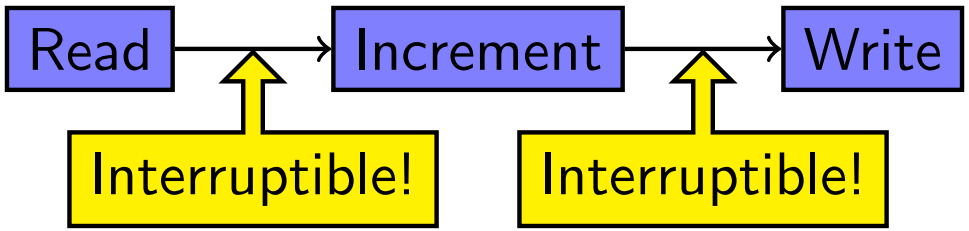

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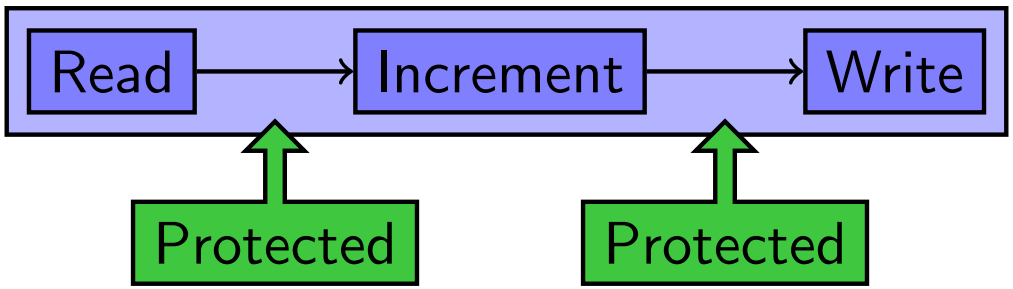

How?

atomic_{add,inc,cmpxchg,...}(int *global, int value);

Questions?

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Image Credits

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